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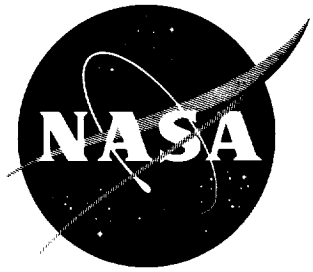

TECHNICAL NOTE

D-1054

A TECHNIQUE FOR INCREASING THE SENSITIVITY OF

A SOLID-STATE FISSION PROBE

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NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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A TECHNIQUE FOR INCREASING THE SENSITIVITY OF A SOLID-STATE FISSION PROBE

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SUMMARY

A small silicon p-n junction wafer, when coated with uranium 235, can be used as a compact fission probe for low power flux and power mapping. Because of the inverse relation between the magnitude of a neutron-induced fission pulse and the inherent capacitance of the detecting element (capacitance is proportional to area), the size, and hence the sensitivity, of the semiconductor detector has been limited. New developments in the field of semiconductor detectors have made it possible to fabricate large area detectors which are essentially free from the capacitance effect. However, preliminary results indicate that they are much more susceptible to radiation damage than the detectors described in this report and as such may not be suitable for flux mapping.

Increasing the sensitivity cannot be accomplished by simply fabricating a larger detector. It has been observed that by combining the silicon p-n junction wafers in a series configuration the capacitance effect can be bypassed, and a fission probe can be made with a resultant increase in sensitivity by a factor of ten while sustaining only a minor decrease in pulse height. Analysis further indicates that for n silicon wafers in series, if $n(C_i + C_c)/C_b \leq 0.1$ where C_i and C_c are the preamplifier input and cable capacitances, respectively, and C_b is the junction capacitance of a single silicon wafer, there should be no substantial reduction in pulse height due to series circuitry.

INTRODUCTION

It was first demonstrated by McKay (ref. 1) in 1949 that a semiconductor could be used to detect charged particles. McKay bombarded the sensitive region (p-n junction) of a semiconductor with a beam of alpha particles traveling parallel to the plane of the p-n junction. Further investigation by Mayer and Gossick (ref. 2) showed that, by forming the p-n junction close to the surface, charged particles could enter perpendicular to the plane of the junction, resulting in a large increase in the sensitive area.

Recently it was reported in reference 3 that a miniature fission probe could be made by coating a diffused junction wafer with uranium 235. Counting efficiencies ranged from 10^{-7} to 10^{-6} counts per neutron per square centimeter. The silicon wafers, each a few square millimeters in area, produced maximum fission pulse heights ranging from 1 to 5 millivolts in inverse proportion to the area coated with uranium 235.

Basically, a solid-state fission probe can be likened to a gaseous ionization chamber in that the voltage pulse produced per incident ionizing particle depends upon the collection of electron-hole pairs which are formed by the passage of the ionizing radiation. While recombination and trapping will occur, a large number of the electron-hole pairs will travel to within a diffusion length of the p-n junction and are separated by the field within the junction to produce a voltage pulse. The pulse thus produced is proportional to the particle energy and inversely proportional to the junction capacitance and the ionization potential of silicon. An obvious way to increase the sensitivity is to enlarge the coated area. However, since the magnitude of the pulse produced per incident fission fragment is inversely proportional to the junction capacitance, any increase in area would necessarily increase the capacitance and thereby reduce the pulse size. Adding more uranium to the detecting surface has little effect since the range of fission fragments in uranium is rather short.

Reference 4 recently reported that by fabricating the semiconductors from high-resistivity silicon, which would allow biasing the detectors, the capacitance effect could be substantially reduced. However, preliminary results indicate that high base resistivity p-n junctions are much more susceptible to radiation damage.

The problem then is to increase the available surface without driving the signal into the noise level. In this report a method is presented supported by analysis and experimental verification, which will be referred to as series circuitry. Using this technique a detector has been constructed consisting of ten silicon p-n junction wafers in series (see fig. 1) with a total area of ~1 centimeter^2, a corresponding thermal neutron sensitivity of 0.90×10^{-3} counts per neutron per square centimeter, and a maximum fission pulse height of 0.75 millivolts.

ANALYSIS OF SERIES CIRCUITRY

Figure 2(a) shows the equivalent circuit of a single silicon p-n junction wafer and the preamplifier input as used in the experiment. The symbols R_b and C_b represent the constituents of the barrier impedance, while R_i and C_i represent the input impedance of the preamplifier. The body resistance R_s of the silicon wafer is obtained from the expression

$$R_s = \frac{l}{A}\rho \qquad (1)$$

where l is the length of the wafer in centimeters, A is the cross-sectional area in square centimeters, and ρ represents the resistivity of the silicon in ohm-centimeters. For the silicon wafer used, a Hoffman 58C (see fig. 3), the body resistance is calculated to be 2.8 ohms. The preamplifier input capacitance is 25 micromicrofarads, and the capacitance C_c of the signal cable leading to the graphite stack has a value of 115 micromicrofarads. The preamplifier input resistance R_i is 1×10^6 ohms, and the barrier capacitance C_b is 3150 micromicrofarads. The resistance of the barrier R_b can be obtained from the following expression for R_T, which is the resultant of the parallel combination of the barrier and preamplifier input resistances:

$$R_T = \frac{R_b R_i}{R_b + R_i} = \frac{\tau}{C_P} \tag{2}$$

where $C_P = C_i + C_c + C_b$ and τ is the time constant of the pulse (see fig. 4). By solving for R_b from equation (2), the barrier resistance is 3.4×10^4 ohms.

Before considering the effect on the pulse amplitude of placing n silicon wafers in series, the factors that affect the magnitude of a pulse from a single silicon wafer will be considered. Since $R_s \ll R_i$, any voltage drop across R_s will be negligible. Also, R_T is large enough that the time constant $R_T C_P$ does not permit appreciable charge to leak during the rise time of the pulse. Consequently, as far as pulse height is concerned, the resistances can be eliminated from the equivalent circuit, and figure 2(b) then represents the circuit for a single silicon p-n junction wafer. If n silicon wafers are now arranged in series across the preamplifier input, figure 2(c) represents the equivalent circuit which will predict the maximum pulse height V_n at the preamplifier input. Suppose that the passage of a fission fragment in one of the silicon wafers results in the separation of a charge q_0 by the electric field of the barrier. Then this charge is shared between the barrier capacitance C_b of the silicon wafer in question and the effective capacitance C_s (see fig. 2(d)) where

$$C_s = \frac{1}{\frac{n-1}{C_b} + \frac{1}{C_i + C_c}} \tag{3}$$

which is the series combination of the other $n - 1$ barrier capacitances and the preamplifier input plus cable capacitance. Then

$$V_n = \frac{q_s}{C_i + C_c} = \frac{q_0 C_s}{(C_s + C_b)(C_i + C_c)} \tag{4}$$

where q_s is the charge on the capacitance C_s. The maximum pulse height V_n is easily shown to be

$$V_n = \frac{V_0 C_P}{n(C_i + C_c) + C_b} \qquad (5)$$

where $V_0 = q_0/C_P$ is the amplitude of the pulse from a single silicon p-n junction wafer. Figure 5 shows the reduction in pulse height as a function of the number of silicon wafers in series as obtained from equation (5).

EXPERIMENTAL ARRANGEMENTS AND RESULTS

The thermal neutron sensitivity (counts/sec/unit flux) of a single silicon wafer was determined in the following manner. The active surface of a wafer was coated with 2 milligrams per square centimeter of uranium 235, and with its signal lead was enclosed in an aluminum tube. The tube was then inserted in a calibrated graphite stack (3 in. from a polonium-beryllium neutron source) and the pulse output of the wafer was amplified by a Tektronix 121 preamplifier and then fed into a Baird Atomic 215 amplifier and 101B scaler. The spectrum of fission pulses obtained from the silicon wafer is shown in figure 4. The maximum fission pulse height is 1 millivolt, with a time constant of ~110 microseconds and a rise time of less than 1 microsecond. A count rate of 10.2±0.2 counts per minute was obtained (extrapolation of integral pulse height curve to zero pulse height). The thermal flux in the graphite stack at the point of measurement was 1.89×10^3 neutrons per square centimeter per second; thus the sensitivity of a Hoffman 58C silicon wafer is 0.90×10^{-4} counts per neutron per square centimeter. This is in good agreement with the calculated value for the sensitivity when considering that no attempt was made to carefully control the uniformity of the uranium 235 coating on the wafer.

In order to examine the effect of series circuitry on maximum pulse height a single silicon wafer, then five, and finally ten in series were placed in the graphite stack. The results are plotted in figure 5.

The proportional increase in count rate as a result of the series technique was observed by mounting first one and then ten detectors in series on the outside of the NASA Zero Power Reactor. Counting equipment used was the same as in the initial calibration. In figure 6 the integral pulse distribution is shown for a single wafer and ten in series.

The effective capacitance of the silicon wafers in series was determined by direct substitution. A 1-millivolt fission pulse was simulated by a pulse generator, and nine silicon wafers were placed in series with the output of the generator. The effect of the wafers on the pulse amplitude was noted, and the experiment was repeated with a calibrated capacitor in place of the silicon wafers. It was then determined what capacitance would be required to produce the same effect on the pulse height as

that of the silicon wafers. (The assumption made here that the series effect on pulse height is mainly capacitance in nature was justified in the analysis.) The measured capacitance of the equivalent of nine silicon wafers in series with the pulse generator was 350 micromicrofarads. Thus a single wafer has an effective barrier capacitance of 3150 micromicrofarads.

CONCLUSIONS

By placing the silicon p-n junction wafers in series it is possible to fabricate large area (~1 cm^2) semiconductor fission detectors. The series technique allows an increase in sensitive area by a factor of at least ten with a proportional increase in fission rate.

Analysis indicates that it is possible to place many more than ten wafers in series. When $n(C_i + C_c)/C_b < 0.1$ (where C_i and C_c are preamplifier input and cable capacitances, respectively, and C_b is the junction capacitance of a single silicon wafer), only a negligible decrease in pulse height will occur. Whether this ratio is always obtainable in practice will depend on the number of wafers in series, the input capacitance of the preamplifier, and its proximity to the detector. Space limitations may determine whether low-capacitance cable can be employed to further reduce the capacitance effect.

The series approach, while being relatively simple, fulfills the present need for a small compact fission probe with a reasonably high sensitivity.

Lewis Research Center
National Aeronautics and Space Administration
Cleveland, Ohio, June 6, 1961

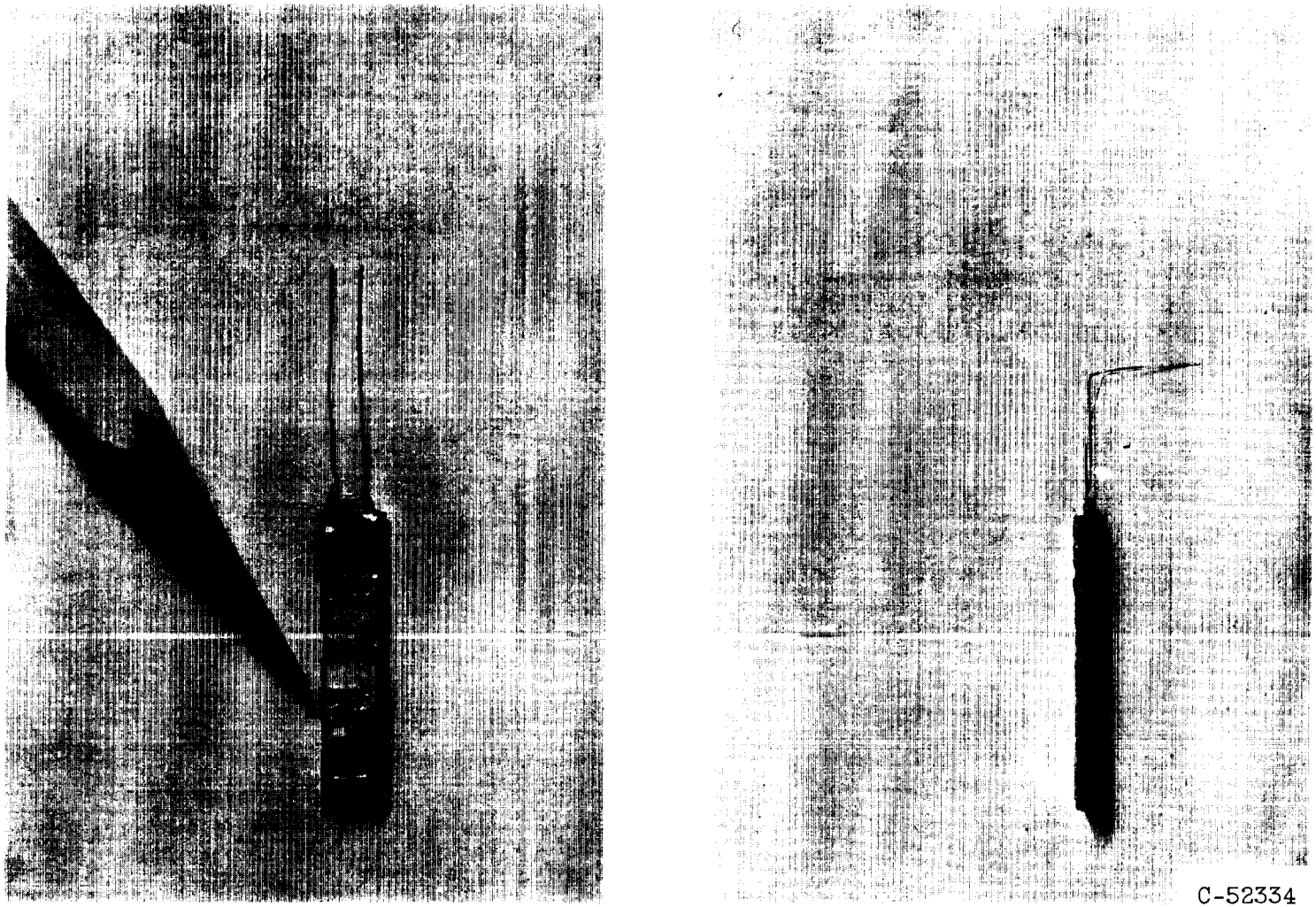
REFERENCES

1. McKay, Kenneth G.: A Germanium Counter. Phys. Rev., vol. 76, no. 10, Nov. 15, 1949, pp. 1537-1538.

2. Mayer, J., and Gossick, B.: Use of Au-Ge Broad Area Barrier as Alpha-Particle Spectrometer. Rev. Sci. Instr., vol. 27, no. 6, June 1956, pp. 407-408.

3. Babcock, R. V., et al.: Coated Semiconductor Is Tiny Neutron Detector. Nucleonics, vol. 17, no. 4, Apr. 1959, pp. 116-122.

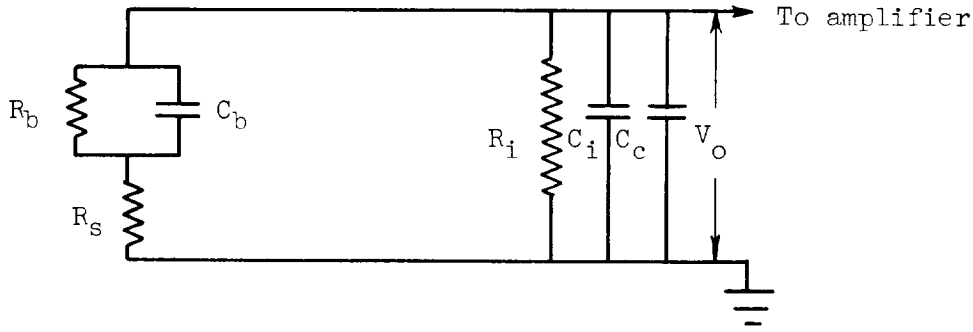
4. Friedland, Stephen S., Mayer, James W., and Wiggins, John A.: The Solid State Ionization Chamber. TM-626, Radiation Phys. Dept., Hughes Aircraft., Jan. 8, 1960.



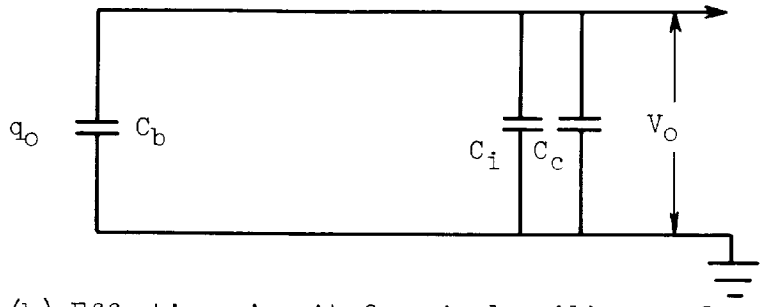
Front view

Side view

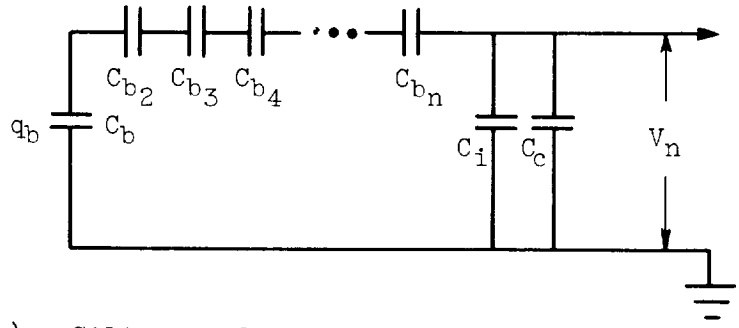
Figure 1. - Solid-state detector utilizing series circuitry.



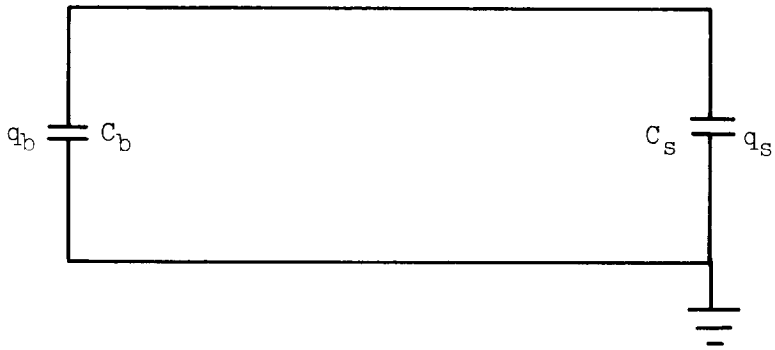
(a) Single silicon wafer and preamplifier input.



(b) Effective circuit for single silicon wafer and preamplifier input.



(c) n Silicon wafers in series and preamplifier input.



(d) Effective circuit for n silicon wafers in series and preamplifier input.

Figure 2. - Equivalent circuit for silicon p-n junction wafers and preamplifier input.

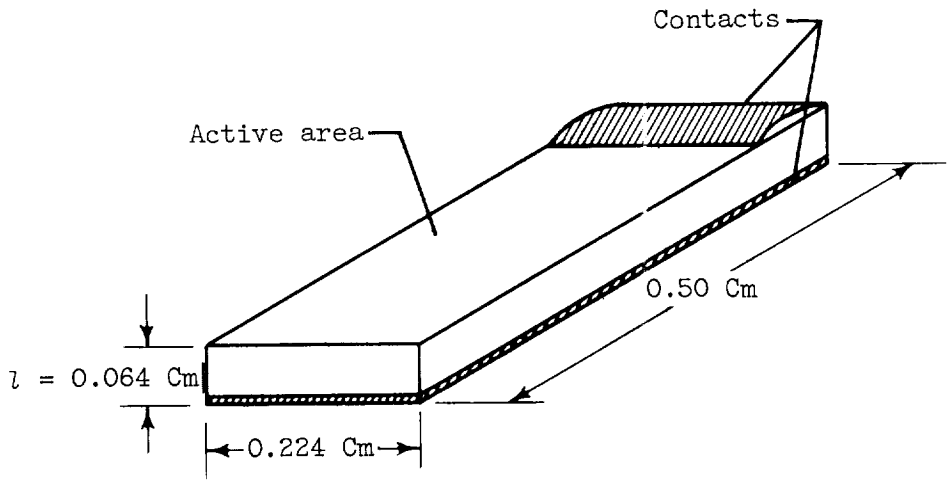
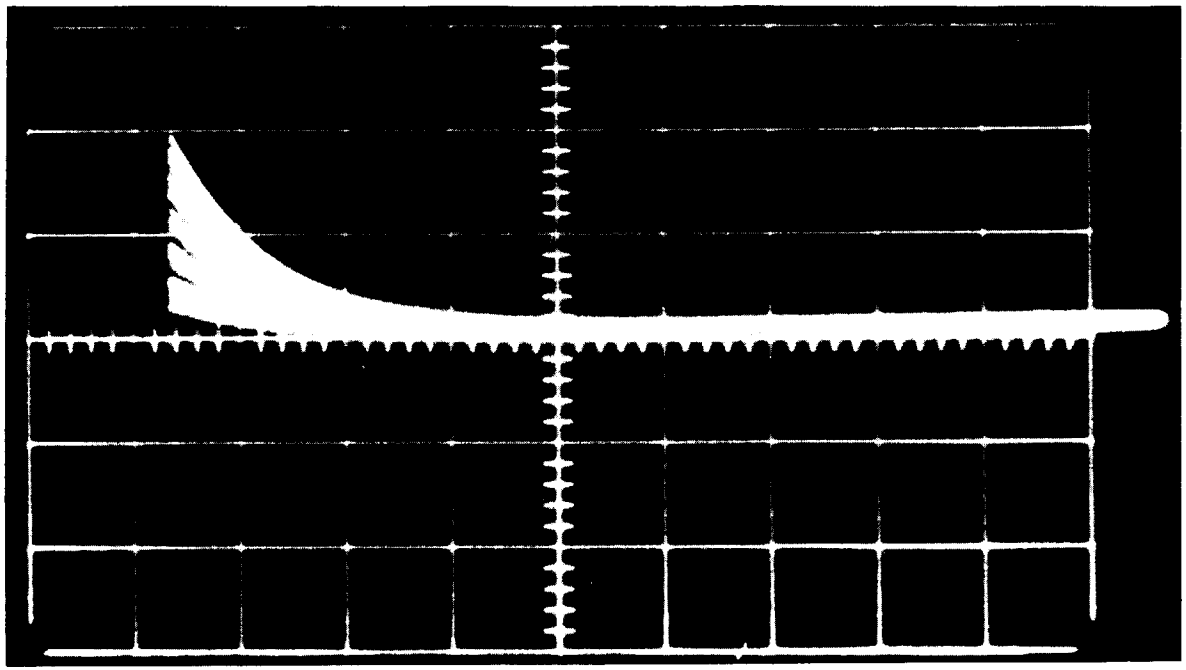


Figure 3. - Single Hoffman 58C silicon p-n junction wafer.



0.50 Millivolt/cm

C-56702

100 Microsec/cm

Figure 4. - Envelope of fission pulses from single Hoffman 58C silicon p-n junction wafer.

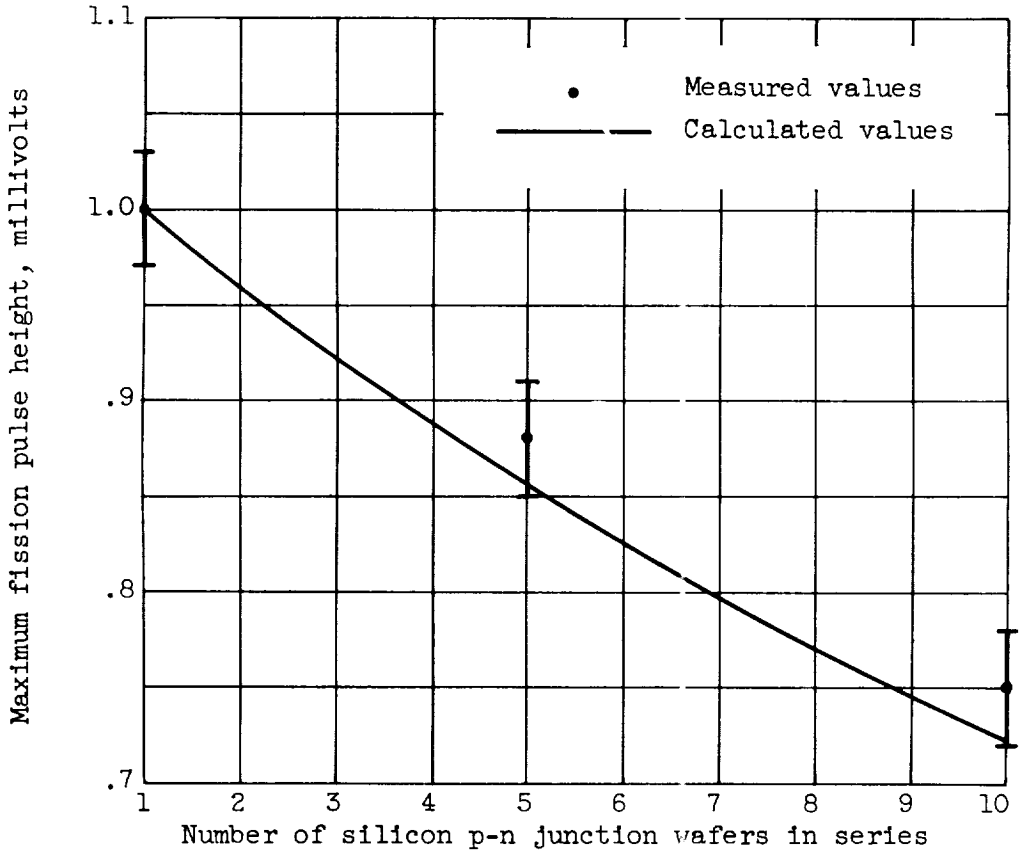


Figure 5. - Calculated and experimental values for maximum fission pulse height as function of number of silicon wafers in series.

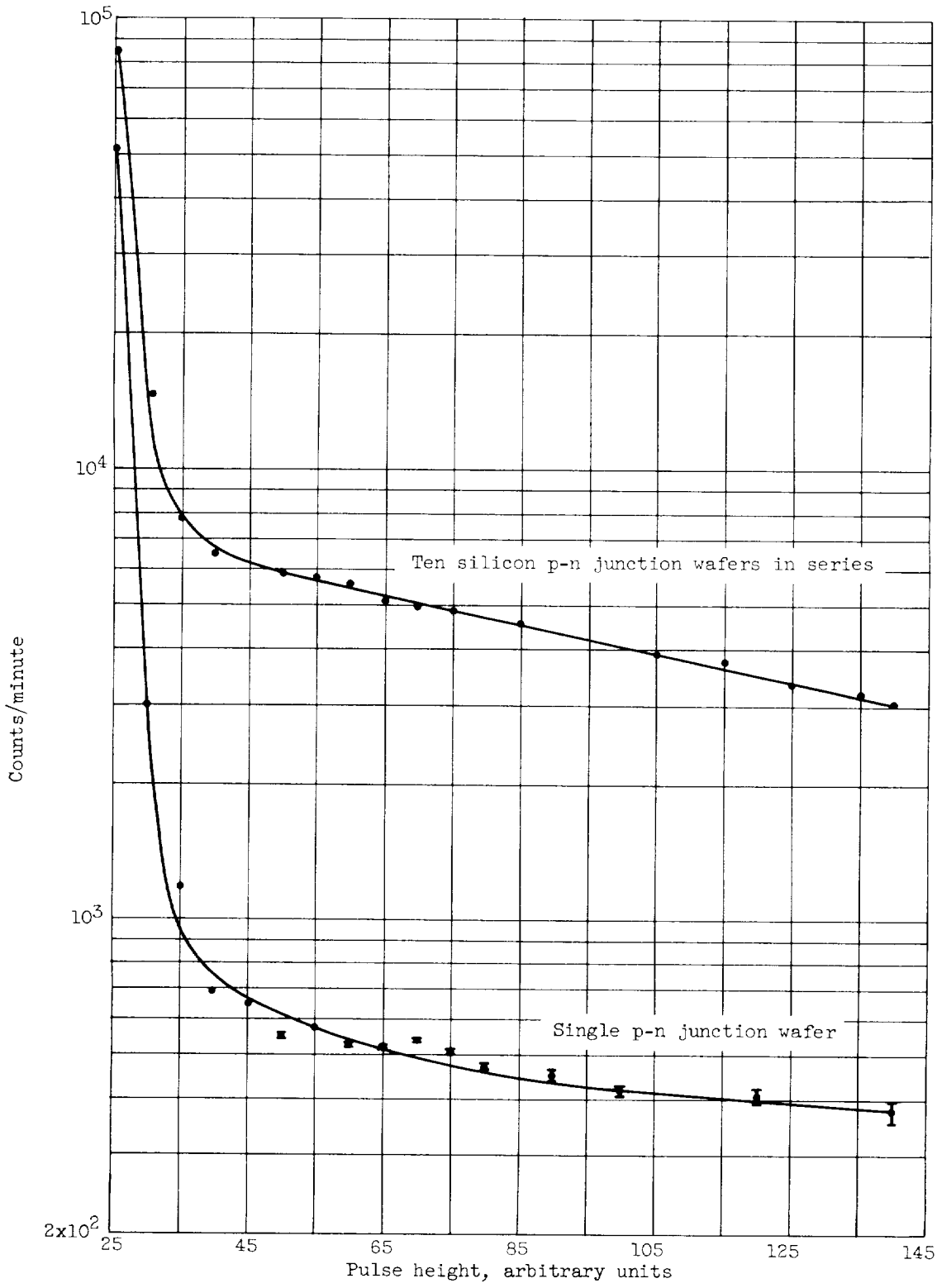


Figure 6. - Counting rate as function of pulse height for fission fragments from silicon p-n junction wafers.